

FIG. 2

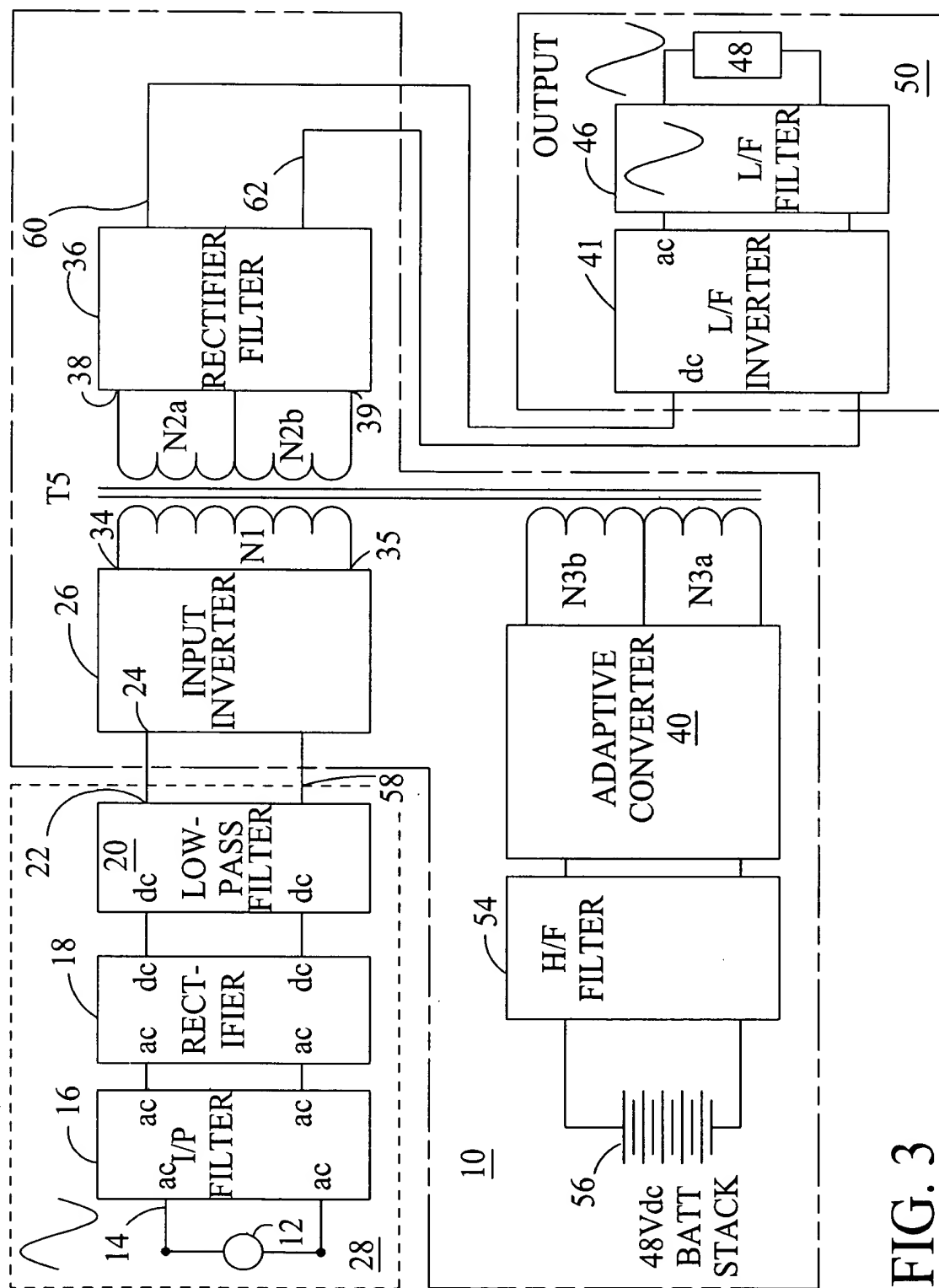


FIG. 3

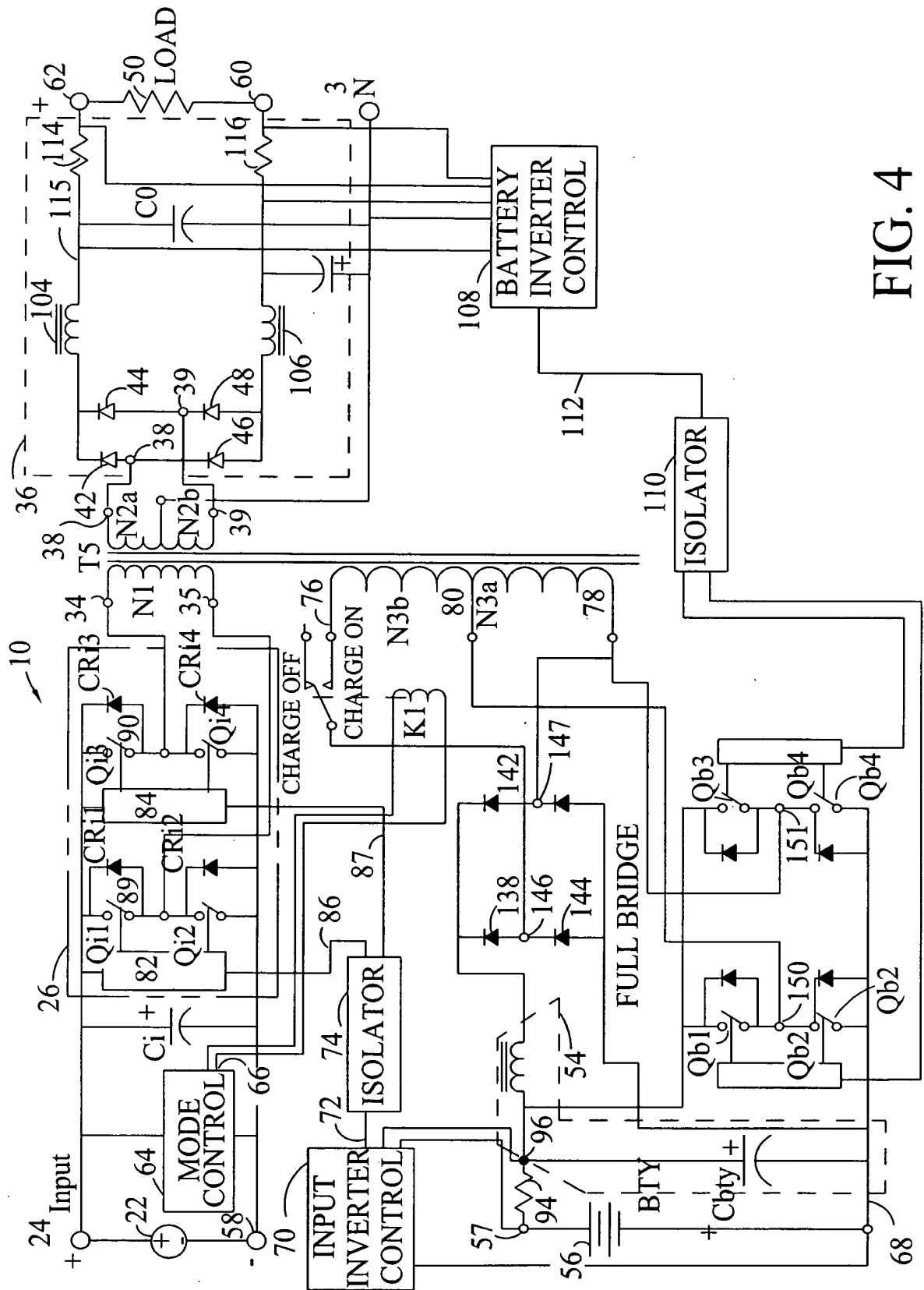


FIG. 4

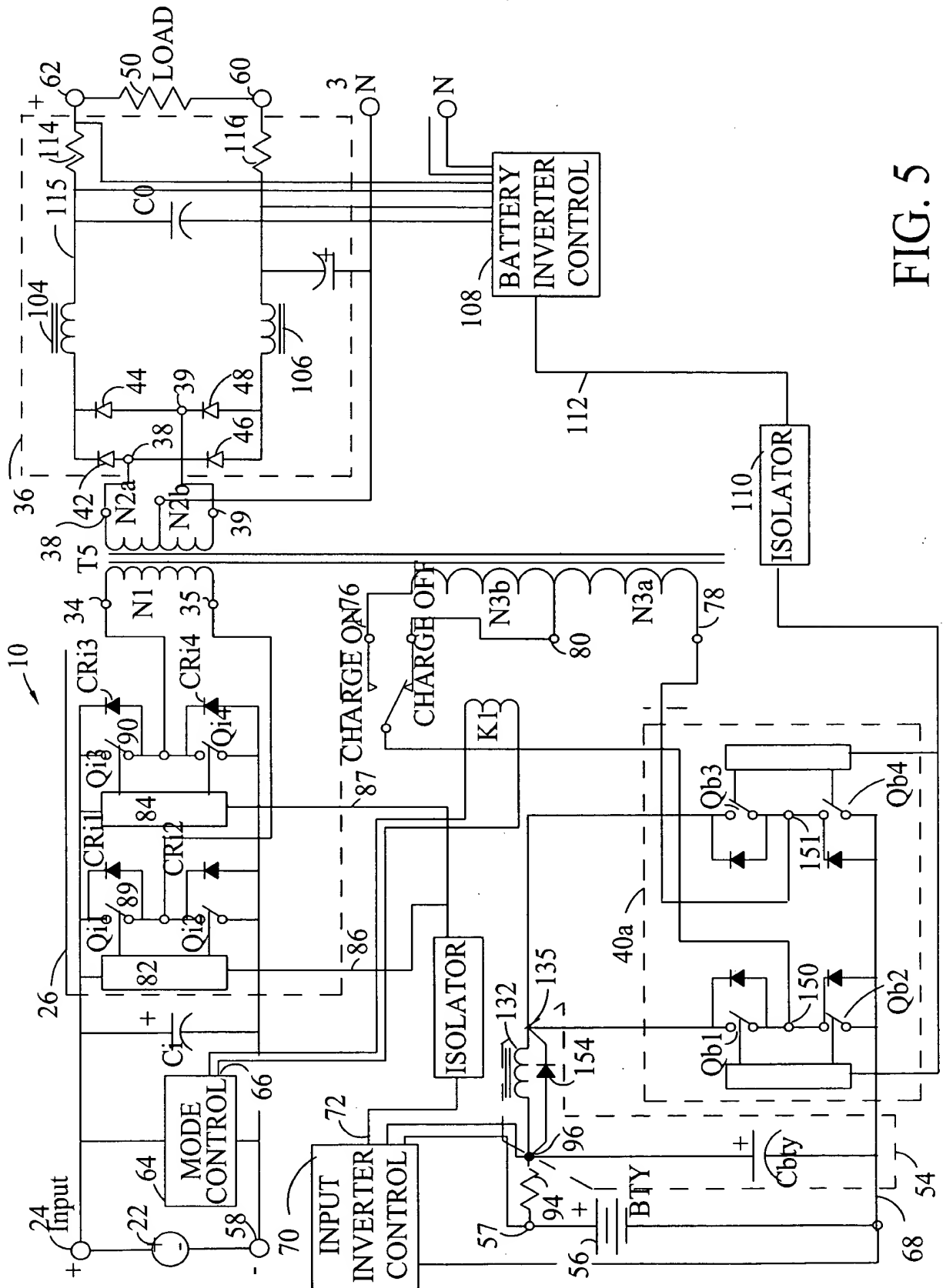


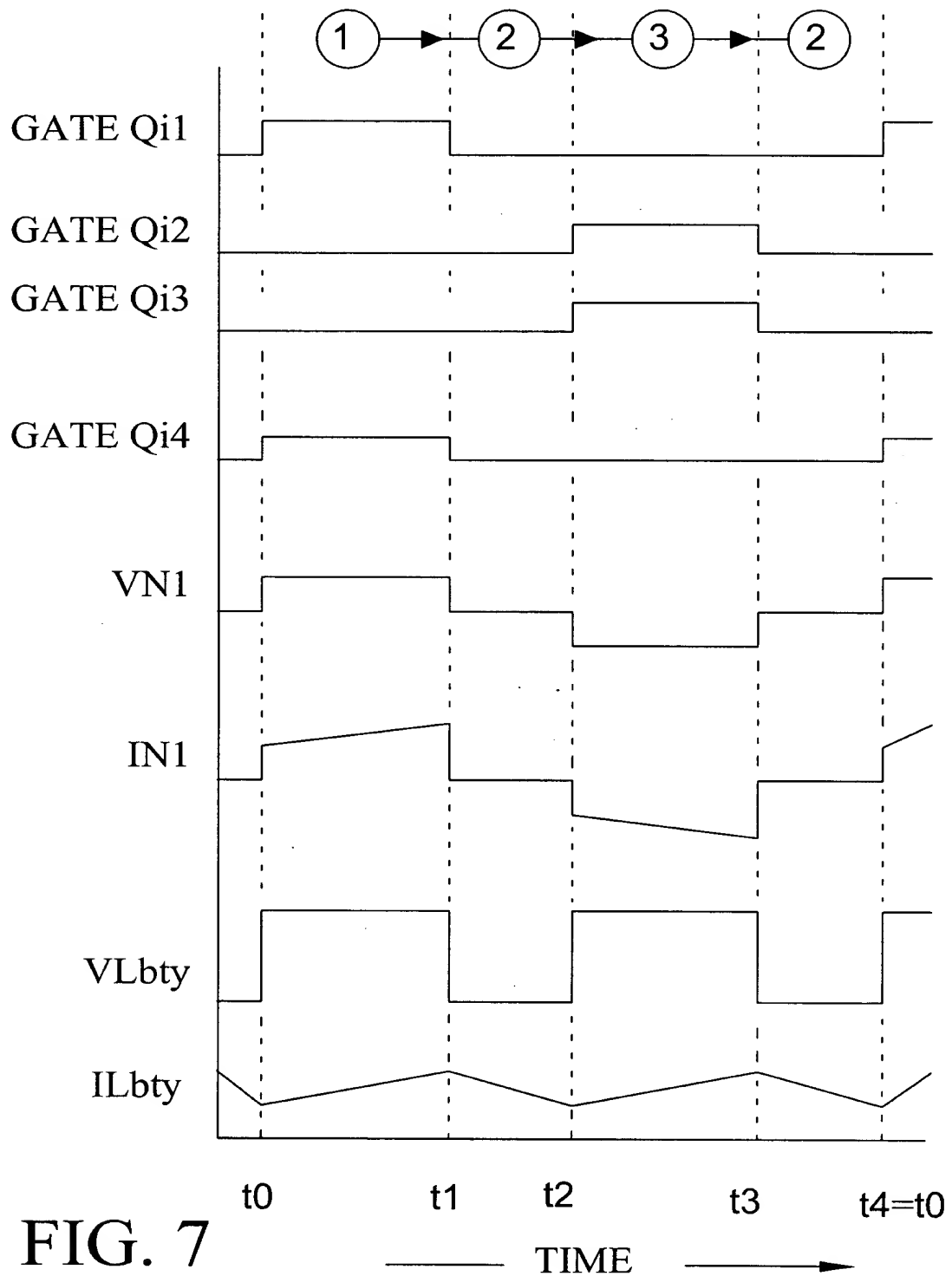
FIG. 5



FIG. 6

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STATE
WHILE INPUT PRESENT



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	ON	OFF
STATE 1:	1;4	2,3
STATE 2:		1;2;3;4
STATE 3:	2;3	1;4

FIG. 8

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STATE
WHILE INPUT ABSENT

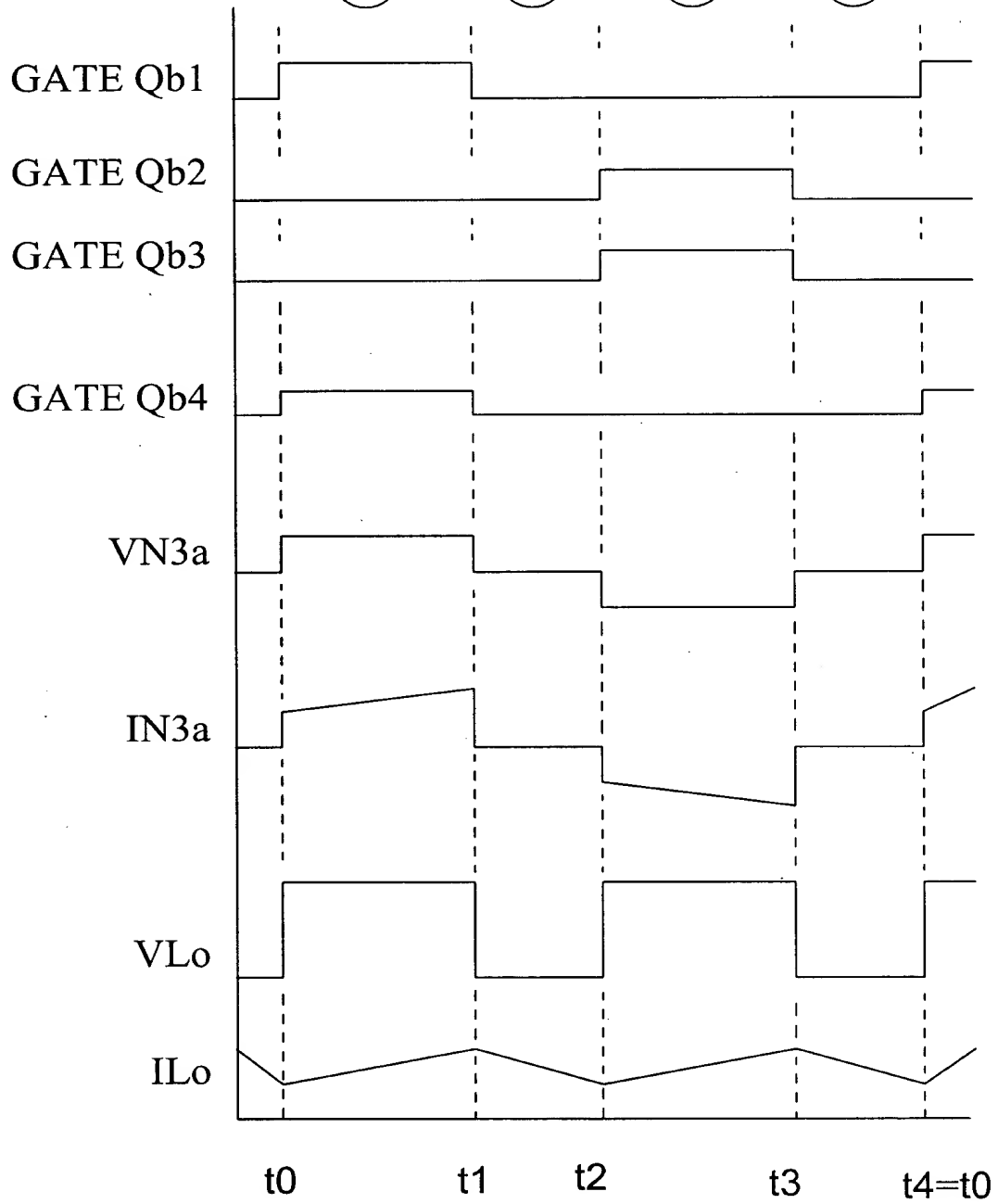
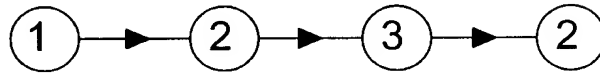
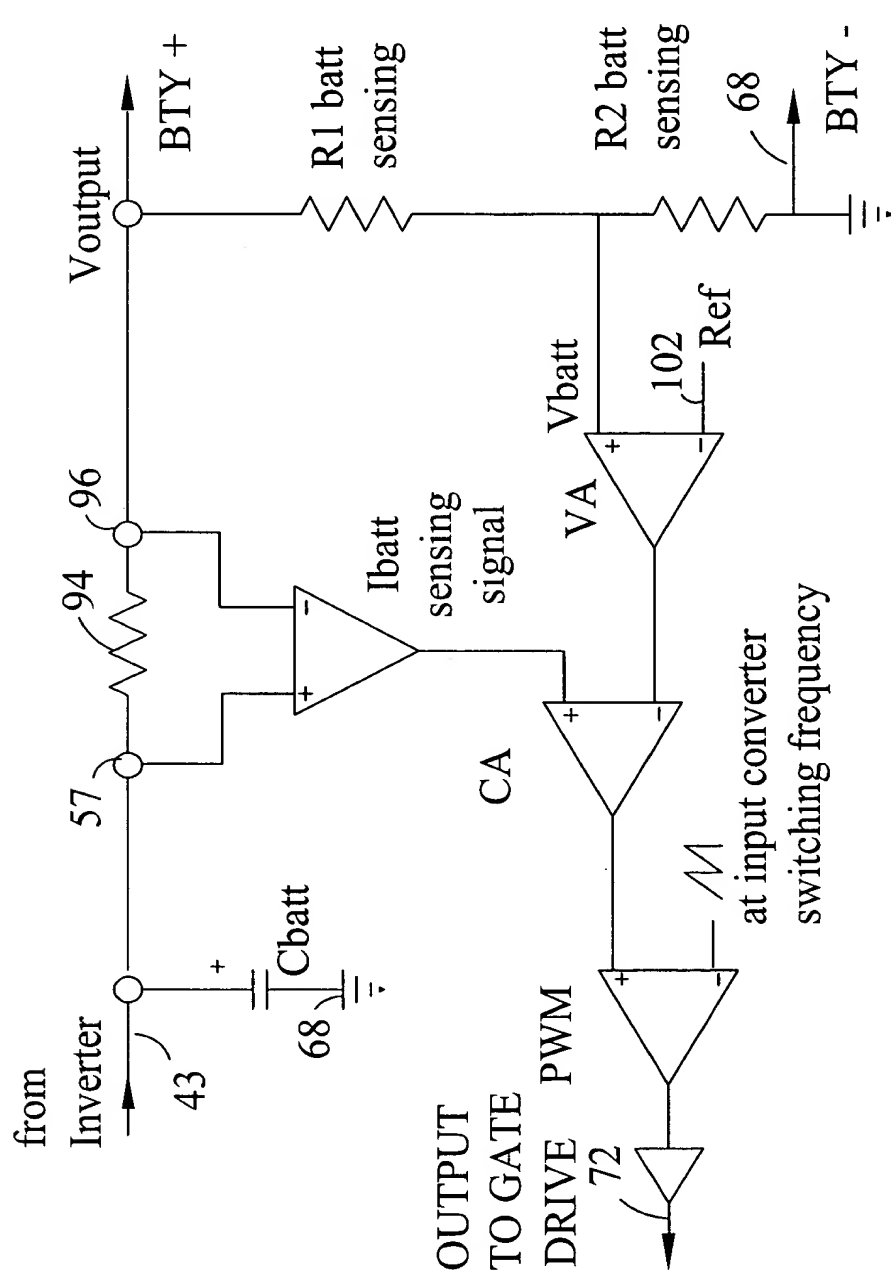
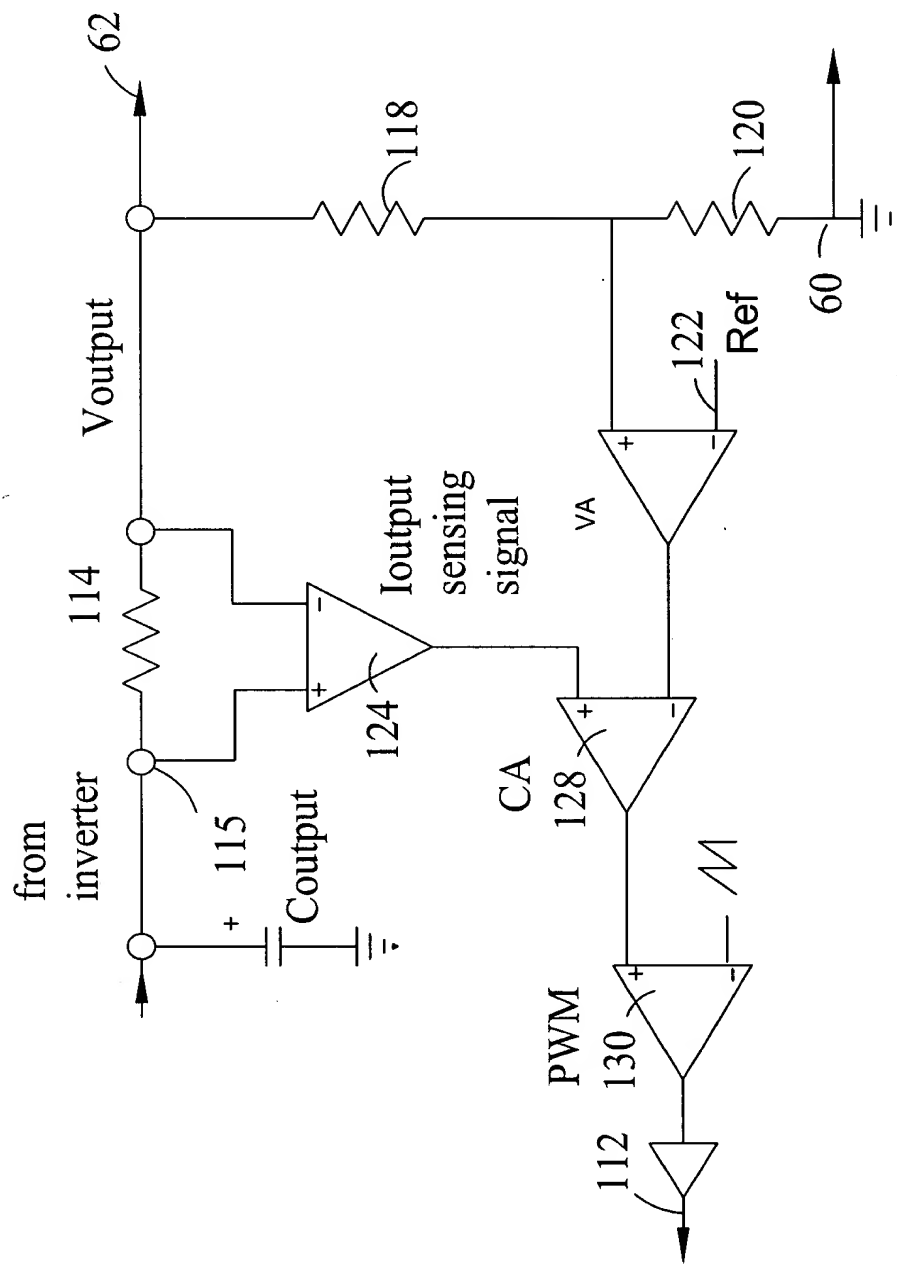


FIG. 9

— TIME —→



INPUT INVERTER CONTROL SCHEMATIC
FIG. 10



BATTERY INVERTER CONTROL SCHEMATIC

FIG. 11



